SCAN CHAIN VERIFICATION USING SYMBOLIC SIMULATION

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ABSTRACT OF THE DISCLOSURE

[056] A method and apparatus for improved formal scan chain equivalence checking to verify the operation of components in a VLSI integrated circuit is described in connection with using symbolic simulation for verification of scan chain equivalency between different modeling representations of a circuit-under-test. The present invention enhances previous techniques by loading each scannable state-element in the circuit design with a symbolic expression that characterizes the logical location of the element and performing a scan shift operation to verify the contents of each scannable state-element at the scan-out and other primary output pins of the design.